ABSTRACT OF THE DISCLOSURE

An improved memory cell architecture is provided herein for reducing, or altogether eliminating, chip-level routing congestion in System-on-Chip environments. Though only a few embodiments are provided herein, features common to the described embodiments include: the formation of bitlines in a lower-level metallization layer of the memory array, and the use of word lines and ground supply lines, both formed in inter-level metallization layer(s) of the memory array, for effective shielding of the bitlines against routing signals in the chip-level routing layer.